AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A programmable logic device, comprising:

configurable logic configured with a pattern generator, the pattern generator configured for a test mode;

a configurable input/output interconnect coupled to the configurable logic;

transceivers coupled to the configurable input/output interconnect; and

the configurable input/output interconnect configured to communicate test signals from the pattern generator for transmission by at least one transceiver of the transceivers;

wherein the configurable logic is configurable responsive to at least one bitstream to define logic functions to provide the pattern generator.

2. (Original) The programmable logic device, according to claim 1, wherein the test mode is a Time Domain Transmissivity mode.

3. (Original) The programmable logic device, according to claim 1, wherein the test mode is a Time Domain Reflectometry mode.

4. (Original) The programmable logic device, according to claim 1, further comprising memory coupled to the pattern generator, the memory having stored therein test pattern information for the pattern generator.

5. (Original) The programmable logic device, according to claim 4, further comprising a pattern detector for a bit error rate testing.

6. (Currently Amended) A method for testing a signal channel, comprising:

coupling a first programmable logic device to the signal channel;

configuring programmable logic of the first programmable logic device

responsive to at least one configuration bitstream to define logic functions to send test signals over the signal channel;

coupling a second programmable logic device to the signal channel to receive the test signals;

configuring programmable logic of the second programmable logic device for a test mode responsive to at least one configuration bitstream to define logic functions to process the test signals, the second programmable logic device configured to test transmissivity of the test signals; and

reconfiguring the programmable logic of the first programmable logic device and the second programmable logic device for at least one of another test mode and an operational mode while coupled to the signal channel.

7. (Original) The method, according to claim 6, further comprising:

coupling the first programmable logic device and the second programmable logic device to one another via another signal channel; and

communicating the test signals over the signal channel and the other signal channel simultaneously to test for cross-talk.

8. (Currently Amended) A programmable logic device, comprising:

configurable logic configured with a pattern detector, the pattern detector configured for a test mode;

a configurable input/output interconnect coupled to the configurable logic;

transceivers coupled to the configurable input/output interconnect; and

the configurable input/output interconnect configured to communicate test signals received by at least one transceiver of the transceivers to the pattern detector;

wherein the configurable logic is configurable responsive to at least one bitstream to define logic functions to provide the pattern generator.

9. (Original) The programmable logic device, according to claim 8, further comprising a test pattern accessible by the pattern detector, the pattern detector

configured to compare the test signals to the test pattern to produce test data therefrom.

10. (Original) The programmable logic device, according to claim 9, wherein the test mode is a bit error rate test mode.

11. (Original) The programmable logic device, according to claim 10, further comprising memory coupled to the pattern detector to receive the test data for storage.

12. (Original) The programmable logic device, according to claim 11, further comprising a processor coupled to the memory for obtaining the test data and configured to process the test data to provide a bit error rate.

13. (Original) The programmable logic device, according to claim 11, wherein the programmable logic device is configurable for another test mode while coupled to a signal channel.

14. (Currently Amended) A channel test system, comprising:

a programmable logic device having programmable logic; and

configuration memory coupled to the programmable logic device, the configuration memory for storing applications for channel testing, the applications for channel testing for configuring the programmable logic device to perform ~~a~~ respective test operations;

wherein the programmable logic is configurable responsive to at least one bitstream stored in the configuration memory to define logic functions to perform the respective test operations.

15. (Original) The channel test system, according to claim 14, wherein at least an application of the applications for channel testing is for configuring the programmable logic with a pattern generator.

16. (Original) The channel test system, according to claim 14, wherein at least an application of the applications for channel testing is for configuring the programmable logic with a pattern detector.

17. (Original) The channel test system, according to claim 14, wherein at least an application of the applications for channel testing is for a Time Domain Reflectometry mode.

18. (Original) The channel test system, according to claim 14, wherein at least an application of the applications for channel testing is for a Time Domain Transmissivity mode.

19. (Original) The channel test system, according to claim 14, wherein at least an application of the application for channel testing is to configure the programmable logic to provide an incident wave.

20. (Original) The channel test system, according to claim 14, wherein the programmable logic device comprises transceivers, at least one of the transceivers configured to provided a controlled edge rate signal.

21. (Original) The channel test system, according to claim 14, wherein the programmable logic device comprises transceivers, at least one of the transceivers configured to provide a variable threshold voltage for sampling.

22. (Original) The channel test system, according to claim 14, wherein at least an application of the applications for channel testing is for a bit error rate test mode.

23. (Currently Amended) A method for testing a signal channel, comprising:
coupling a first programmable logic device to the signal channel;
configuring the first programmable logic device to send test signals over the

signal channel;

coupling a second programmable logic device to the signal channel to receive the test signals;

configuring the second [[first]] programmable logic device for a test mode to measure reflected versions of the test signals; and

reconfiguring the first programmable logic device and the second programmable logic device for another test mode while coupled to the signal channel;

wherein the first programmable logic device and the second programmable logic device are configurable and reconfigurable responsive to bitstreams to define logic functions for the test mode and the other test mode.

24. (Original) The method, according to claim 23, further comprising:

coupling the first programmable logic device and the second programmable logic device to one another via another signal channel; and

communicating the test signals over the signal channel and the other signal channel simultaneously to test for cross-talk.